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2661	

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Please find below and/or attached an Office communication concerning this application or proceeding.

	Application No.	Applicant(s)
Office Action Summary	09/686,178	BROWN ET AL.
	Examiner	Art Unit
	Ian N Moore	2661

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE _3_ MONTH(S) FROM
THE MAILING DATE OF THIS COMMUNICATION.
- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed
  after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
  Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any
  earned patent term adjustment. See 37 CFR 1.704(b).

Status

1) ☒ Responsive to communication(s) filed on *the amendment filed on 6-14-2004* .

2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.

3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is
   closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4) ☒ Claim(s) *1-18* is/are pending in the application.

    4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5) ☐ Claim(s) _____ is/are allowed.

6) ☒ Claim(s) *1-9,11,13-15,17* is/are rejected.

7) ☒ Claim(s) *10,12,16 and 18* is/are objected to.

8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9) ☐ The specification is objected to by the Examiner.

10) ☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

    Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

    Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

    a)☐ All b)☐ Some * c)☐ None of:

        1.☐ Certified copies of the priority documents have been received.

        2.☐ Certified copies of the priority documents have been received in Application No. _____ .

        3.☐ Copies of the certified copies of the priority documents have been received in this National Stage
           application from the International Bureau (PCT Rule 17.2(a)).

    * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)

2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)

3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
    Paper No(s)/Mail Date _____ .

4) ☐ Interview Summary (PTO-413)
    Paper No(s)/Mail Date. _____ .

5) ☐ Notice of Informal Patent Application (PTO-152)

6) ☐ Other: _____ .

DETAILED ACTION

Response to Amendment

1. Claim objection, on claim 8 is withdrawn since they are being amended accordingly.

2. New claims 14-18 are added.

Response to Arguments

3. Applicant's arguments filed on 6-14-2004 regarding claims 1-9,11,13-15, and 17 have been fully considered but they are not persuasive.

Regarding claims 1-3, the applicant argued that, "…Applicants contend that Riley teaches a network interface for multiplexing a multi-bit message across a bit level network to a preselected one of a plurality of time-division multiplexed addresses **at a rate of one message bit per consecutive data frame until the complete multi-bit message has been transmitted** …" in page 11, lines 2-5.

In response to applicant's argument, the examiner respectfully disagrees that Riley does not teaches a network interface for multiplexing a multi-bit message across a bit level network to a preselected one of a plurality of time-division multiplexed addresses. Riley'539 discloses an apparatus (see FIG. 1) for transferring multiplexed multiple multi-bit messages across a bit level network (see col. 6, line 40-52; note the system is able to transfer the multi-bits of data), said apparatus comprising: a network interface for accessing the bit level network (see FIG. 1, Conductors 40), said network interface configured to transmit and receive a message at a preselected one of a plurality of time-division multiplex addresses (see FIG. 21, Frame Identifiers/addresses in plurality of frames/messages) on each channel of a

preselected channel set (see FIG. 21, pluralities of serial multiplex time division slots (i.e.

channels) forms into a frame (i.e. pre-selected channel set); see col. 5, line 2-65; see col. 16,

line 54 and col.17, line 24; note that after multiplexing the time slots, each frame is given a

predefined/unique frame number. The conductors/buses transmit and receive the frames.)

In response to applicant's argument that the references fail to show certain features

of applicant's invention, it is noted that the features upon which applicant relies (i.e.,

transmitting at a rate of one message bit per consecutive data frame until the complete

multi-bit message has been transmitted) are not recited in the rejected claim(s). Although

the claims are interpreted in light of the specification, limitations from the specification are

not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir.

1993).

The applicant argued that, "...Riley's frames are not equivalent to, nor do they

function in the same manner as the preselected channel sets..." in page 11, lines 8-9, 20-22.

In response to applicant's argument, the examiner respectfully disagrees that

Riley's frames are not equivalent to, nor do they function in the same manner as the

preselected channel sets. As clearly shown in FIG. 21, the time slots (i.e. channels) forms

into a frame. Each frame contains predetermined/predefined 256 time slots or channels. One

set contains a predefined 256 of channels/timeslots. Thus, a frame is a preselected channel

set; see col. 5, lines 2-65, see col. 16, lines 54 and see col. 17, lines 24.

The applicant argued that, "... Riley's Frame identifiers are addresses of the present

invention; time division slots are the channels of the present invention, which is not

absolutely true in either case..." in page 11.

In response to applicant's argument, note that applicant is only claiming,

"**addresses on each channel**", and there is <u>no</u> specific limitation regarding the address or

channel. Each frame has plurality of timeslots or channels, and each frame has the frame ID

that is the address of the frame. Note that "timeslots" and "channels" are interchangeable use

in the art when determining/referring what consists in a frame. Thus, examiner asserts

Riley'539 teaches addresses (see FIG. 21, Frame Identifiers/addresses in plurality of

frames/messages) on each channel of a preselected channel set (see FIG. 21, pluralities of

serial multiplex time division slots (i.e. channels).

The applicant argued that, "…Riley's frames are not equivalent to, nor do they

function in the same manner as the preselected channel sets…. Each of the 256 bits of Riley's

frame represent one address, while **each channel of a channel set of the present invention**

is made up of some number of bits (16 or 32 bits in the representative embodiment)

assigned to one address…" in page 11.

In response to applicant's argument that the references fail to show certain features

of applicant's invention, it is noted that the features upon which applicant relies (i.e., **each**

channel of a channel set is made up of some number of bits (16 or 32 bits in the

representative embodiment) assigned to one address) are not recited in the rejected

claim(s). Although the claims are interpreted in light of the specification, limitations from

the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26

USPQ2d 1057 (Fed. Cir. 1993).

The applicant argued that, "... however, it receives a multi-bit message at a rate of one bit per frame until the shift register is full, it does not **receive a complete multi-bit message on a preselected channel set...**" in page 11.

In response to applicant's argument that the references fail to show certain features of applicant's invention, it is noted that the features upon which applicant relies (i.e., **receive a <u>complete</u> multi-bit message**) are not recited in the rejected claim(s). Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993).

Regarding claim 2, the applicant argued that, "...applicants agree that Riley'539 likely does teach a network interface having a clock signal and a data signal..." in page 12.

In response to applicant's argument, the examiner respectfully disagrees that the Riley'539 likely does teach a network interface having a clock signal and a data signal. Riley'539 discloses wherein said network interface includes a clock signal and a data signal (see FIG. 1, the conductors 40 consists of master clock line/bus 44 and data bus 46; see col. 5, line 30-45)

Regarding claim 3, the applicant argued that, "...it is not sent in a data stream of **consecutive data bits** as in the present invention..." in page 12.

In response to applicant's argument that the references fail to show certain features of applicant's invention, it is noted that the features upon which applicant relies (i.e., **sending consecutive data bits**) are not recited in the rejected claim(s). Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993).

    Regarding claims 4-9,11,13, the applicant argued that, "…the teaching of

Sakagami relies on bit stream transmission of data, which is not taught, suggested or

supported by bit level multiplexing of Riley'539…" in page 12.

    In response to applicant's argument, the test for obviousness is not whether the

features of a secondary reference may be bodily incorporated into the structure of the primary

reference; nor is it that the claimed invention must be expressly suggested in any one or all of

the references. Rather, the test is what the combined teachings of the references would have

suggested to those of ordinary skill in the art. See *In re Keller*, 642 F.2d 413, 208 USPQ 871

(CCPA 1981). In particular, Riley'539 discloses multi-bit level network, see col. 6, line 40-

52. As stated by the applicant, Sakagami'525 discloses bit stream transmission of data. As

stated in claim rejection below, the purpose of utilizing Sakagami'525 is not to bodily replace

one system with other, instead the teaching or concepts of Sakagami'525 is utilized. Thus, the

combination is proper.

    Regarding claims 4-9,11,13, the applicant argued that, "…Applicants do not

believe that theses elements, as defined by Sakagami'525, teach or suggest the "command

segment" as claimed in the present invention…none of the element of Sakagami'525 teach or

suggest what is to be done with data provided in the "operand segment"…" in page 13.

    In response to applicant's argument that the references fail to show certain features

of applicant's invention, it is noted that the features upon which applicant relies (i.e., **what is

to be done with data provided in the "operand segment"**) are not recited in the rejected

claim(s). Although the claims are interpreted in light of the specification, limitations from

the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26

USPQ2d 1057 (Fed. Cir. 1993).

In response to applicant's argument, the examiner respectfully disagrees that

Sakagami'525, teach or suggest the "command segment" as claimed in the present invention.

As stated in rejection below, examiner asserts the command as Riley'539 header/control

information bits: HD, ADS, SLP, and AP, see FIG. 3. The function and purpose of command

segment is to control/dictate/manage how data should be processed or function, and the

command segment contains such control information data/bits. The purpose of header/control

information bits (i.e. HD, ADS, SLP, and AP) is to control/dictate/manage how data should

be processed or function, and the command segment contains such control information

data/bits such as HD (to signal the start of the data), ADS (to define the address), SLP (to

define the sleep bit) and AP (to define parity to correct error). Thus, it is clear that

Sakagami'525 discloses the "command segment". Examiner asserts an operand as

Sakagami'525 address ADS, see FIG. 3; col. 6, line 16-64. The control/command bits in

header describes or define what is to be done with the data provided in address

segment/fields.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the

basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

1. Claims 1-3 are rejected under 35 U.S.C. 102(b) as being anticipated by Riley (5,907,539).

Regarding Claim 1, Riley'539 discloses an apparatus (see FIG. 1) for transferring

multiplexed multiple multi-bit messages across a bit level network (see col. 6, line 40-52;

note the system is able to transfer the multi-bits of data), said apparatus comprising:

a network interface for accessing the bit level network (see FIG. 1, Conductors 40),

said network interface configured to transmit and receive a multi-bit message (i.e. each

message that transmits/receives in the system contains more than one bit) at a preselected one

of a plurality of time-division multiplex addresses (see FIG. 21, Frame Identifiers/addresses

in plurality of frames/messages) on each channel of a preselected channel set (see FIG. 21,

pluralities of serial multiplex time division slots (i.e. channels) forms into a frame (i.e. pre-

selected channel set); see col. 5, line 2-65; see col. 16, line 54 and col.17, line 24; note that

after multiplexing the time slots, each frame is given a predefined/unique frame number. The

conductors/buses transmit and receive the frames.)

a processor in communication with said network interface (see FIG. 16, Integrated

circuit 80 which is in communication with conductors (i.e. Data bus 46 and common bus

48));

a memory in communication with said processor (see FIG. 16, Serial to Parallel Shift

Register 496 stores the data, and it couples to Integrated circuit 80); and

a second interface for connecting either an input or an output device (see FIG. 1,

Input Device 50 or Output Device 54) to said processor (see FIG. 16, An output device 54 is

couples to Integrated circuit 80);

whereby the multiple multi-bit messages are transmitted over said network interface

(see FIG. 1, the multiplex data from Data Link modules are transmitted to the conductors 40;

see col. 3, line 65-67).

Regarding Claim 2, Riley'539 discloses wherein said network interface includes a

clock signal and a data signal (see FIG. 1, the conductors 40 consists of master clock line/bus

44 and data bus 46; see col. 5, line 30-45).

Regarding Claim 3, Riley'539 discloses wherein said data signal is a serial data

stream synchronized with the said clock signal (see FIG. 2A, Input clock terminal 84, Input

data terminal 86; note that the serial data signal is synchronized according to the clock

signals. See col. 6, line 21-54 and see col. 15, line 12-62).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all

obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in
section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are
such that the subject matter as a whole would have been obvious at the time the invention was made to a person
having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the
manner in which the invention was made.

2. Claims 4-9,11,13-15, and 17 are rejected under 35 U.S.C. 103(a) as being unpatentable over

Riley'539 in view of Sakagami (5,329,525).

Regarding claim 4, Riley'539 discloses all aspects of the claimed invention set forth in the rejection of claim 1 as described above, and further teaches wherein said data signal includes said multi-bit message.

Riley'539 does not explicitly disclose said message including a command segment and a data segment, said command segment includes at least an operator and an operand.

However, the above-mentioned claimed limitations are taught by Sakagami'525. In particular, Sakagami'525 teaches said message including a command segment (see FIG. 3, header/control information bits: HD, ADS, SLP, and AP) and a data segment (see FIG. 3, data information bits: Rx), said command segment includes at least an operator (see FIG. 3, HD, SLP, and AP) and an operand (see FIG. 3, address ADS). Also see col. 6, line 16-64.

In view of this, having the system of Riley'539 and then given the teaching of Sakagami'525, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the system of Riley'539, by providing a data frame which consists of both command/control/header bits and data bits, as taught by Sakagami'525. The motivation to combine is to obtain the advantages/benefits taught by Sakagami'525 since Sakagami'525 states at col. 3, line 5-40 that such modification would improve the communication and exchange of information between a master station and slave stations.

Regarding claim 5, the combined system of Riley'539 and Sakagami'525 discloses all aspects of the claimed invention set forth in the rejection of claim 1 and 4 as described above. Riley'539 further teaches wherein segment is a serial bitstream starting at a specified address determined by said clock signal on a first channel of said preselected channel set (see

FIG. 17A, address A time slot 422 of the frame 62), and said segment is a serial bitstream

starting at said specified address on a second channel of said preselected channel set (see

FIG. 17B address B time slot 424 of the frame 62). Also, see col. 7, line 65-67; col. 17, line

1-39; col. 5, line 24-65; col. 3, line 55-67; note that the data link has plurality of time

slots/channels (e.g.. Channel A with address A and channel B with address B). Each time slot

is multiplexed and incorporated within a frame, and the frame is identified by a frame

address. The beginning address/cycle of the time slot for transmission is instructed by the

master clock signal.

In addition, Sakagami'525 discloses wherein said command segment and said data

segment starts at said specified address (see FIG. 3, HD, ADS, SLP, AP, RX; see col. 6, line

14-65; note that both header/control and data information are transmitted between the master

station and slave stations. The header/control and data information bits must have a specific

predefined address to start.)

In view of this, having the system of Riley'539 and then given the teaching of

Sakagami'525, it would have been obvious to one having ordinary skill in the art at the time

the invention was made to modify the system of Riley'539, by further assigning specific

addresses to the command/control/header bits to the first portion of the frame, and assign

specific address to the data bits to the second portion of the frame, as taught by

Sakagami'525, for the same motivation as stated above in Claim 4.

Regarding claim 6, the combined system of Riley'539 and Sakagami'525 discloses

all aspects of the claimed invention set forth in the rejection of Claims 1 and 4 as described

above, and Riley'539 further teaches wherein a read request, said memory at a location

specified by said operand contains data which is copied to said data segment (see FIG. 15,

Shift Registers 590 and 588, and FIG. 1, data bus 46 and clock bus 44; see col. 3, line 65-67;

note that in response to the master clock request/instruct signal message, the data link module

retrieves/passes the associated data to the data bus. Thus, the request/instruction signal is the

read signal.)

Sakagami'525 further discloses wherein said operator includes a request (see FIG. 3,

Header/control bits: HD, ADS, SLP and AP; see col. 6, line 5-64; note that when the slave

station receives the DFa frame from the master station, it performs the tasks accordingly).

In view of this, having the system of Riley'539 and then given the teaching of

Sakagami'525, it would have been obvious to one having ordinary skill in the art at the time

the invention was made to modify the system of Riley'539, by further performing

tasks/operations according to the headers/control requests/bits, as taught by Sakagami'525,

for the same motivation as stated above in Claim 4.

Regarding claim 7, the combined system of Riley'539 and Sakagami'525 discloses

all aspects of the claimed invention set forth in the rejection of Claims 1 and 4 as described

above, and Riley'539 further teaches wherein a write request, said data segment contains data

which is copied to said memory at a location specified by said operand (see FIG. 15, Shift

Registers 590 and 588; see col. 3 55-65; note that in response to the master clock

request/instruct signal, the data link module stores the associated data in the specific

corresponding registers. Thus, the request/instruction signal is the write signal message.)

Sakagami'525 further discloses wherein said operator includes a request (see FIG. 3, HD, ADS, SLP and AP; see col. 6, line 5-64; note that when the slave station receives the DFa frame with Rx logic value 0 and parity bit value 1 from the master station, it performs the tasks accordingly).

In view of this, having the system of Riley'539 and then given the teaching of Sakagami'525, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the system of Riley'539, by further performing tasks according to the headers/control requests/bits, as taught by Sakagami'525, for the same motivation as stated above in Claim 4.

Regarding claims 8 and 14, Riley'539 discloses a method for transferring large amounts of complex data between a data link module (see FIG. 1, Data Link Module 32) and a host (see FIG. 1, the combined system of Host computer 34 and Master clock module 36) across a bit level network (see FIG. 1, Conductors 40), said method comprising the steps of:

(a) configuring a channel set having at least two bit level time division multiplexed channels to said data link module (see FIG. 21, each time slot field 85 consists 256 timeslots/channels of a bit level time division channels/timeslots, and at least two channels/time-slots is considered as a channel/timeslot set; see col. 5, line 2-65);

(b) configuring a frame address to said data link module (see FIG. 21, Frame Identifiers/addresses in plurality of frames/messages; see col. 5, line 2-65; see col. 16, line 54 and col. 17, line 24. Note that after multiplexing the time slots, each frame is given a predefined/unique frame number);

(c) sending a multi-bit message (i.e. each message that transmits/receives in the system contains more than one bit) from said host to said data link module, said message including a message segment on a first channel of said channel set at said data link module frame address (see FIG. 17A, address A time slot 422 of the frame 62) and a message data segment on a second channel of said channel set at said data link module frame address (see FIG. 17B address B time slot 424 of the frame 62. Also, see col. 7, line 65-67; col. 17, line 1-39; col. 5, line 24-65, col. 3, line 55-67; note that the data link has plurality of time slots/channels (e.g.. Channel A with address A and channel B with address B). Each time slot is multiplexed and incorporated within a frame, and the frame is identified by a frame address. The beginning address/cycle of the time slot for transmission is instructed by the master clock signal.) said message segment including a register and at least either of a read request or a write request (see FIG. 15, Shift Registers 590 and 588, and FIG. 1, data bus 46 and clock bus 44; see col. 3, line 65-67; note that the request/instruct signal from the master clock must include the output module to store/pass the associated data. Thus, the request/instruction signal is the read/write signal message);

(d) accessing a register in said data link module specified in said register as a specified register (see FIG. 15, Shift Registers 590 and 588; see col. 3 55-65; note that in response to the master clock request/instruct signal, the data link module accesses/stores the associated data in the registers);

(e) sending a message sending a message from said data link module to a bus, said message including a on a first channel of said channel set at said data link module frame address and a segment on a second channel of said channel set at said data link module frame

address (see FIG. 15, Shift Registers 590 and 588, and FIG. 1, data bus 46 and clock bus 44;

see col. 3, line 65-67; note that in response to the master clock request/instruct signal, the

data link module passes the associated data to the data bus. Also, note that the same stored

message information must pass to the data bus.)

Riley'539 does not explicitly disclose

(c) sending a message from said host to said data link module, said message including

a message command segment and a message data segment, said message command segment

including a register operand;

(e) sending a reply from said data link module to said host, said reply including a

reply command segment and a reply data segment.

However, the above-mentioned claimed limitations are taught by Sakagami'525. In

particular, Sakagami'525 teaches (c) sending a message from said host (see FIG. 2, Master

Station 10) to said data link module (see FIG. 2, Slave Station 100), said message including a

message command segment (see FIG. 3, header/control information bits: HD, ADS, SLP, and

AP) and a message data segment (see FIG. 3, data information bits: Rx), said message

command segment including an operand (see FIG. 3, address information ADS); See col. 6,

line 15-54; note that the master station 10 transmits the instruct/request frame DFa to the

addressed slave station 100 in order to perform/operate tasks. The DFa frame consists

header/control information bits and data information bits.

(e) sending a reply (see FIG. 3, DFb frame) from said data link module (see FIG. 2,

Slave Station 100) to said host (see FIG. Master Station 10), said reply including a reply

command segment (see FIG. 3, Data bit t0 is set logical 1, and parity bit and error bit) and a

reply data segment (see FIG. 3, Data bit t1-15 is set logical 0). Also, see col. 6, line 5-15 and

line 55-64. After performing/operating according to the master station's instruction, the slave

station returns the frame DFb back to the master station by setting appropriate

control/command bits and data bits.

In view of this, having the system of Riley'539 and then given the teaching of

Sakagami'525, it would have been obvious to one having ordinary skill in the art at the time

the invention was made to modify the system of Riley'539, by providing a mechanism to

transfers data frames/messages between the master/host and the slave/client, as taught by

Sakagami'525. The motivation to combine is to obtain the advantages/benefits taught by

Sakagami'525 since Sakagami'525 states at col. 3, line 5-40 that such modification would

improve the communication and exchange of information between a master station and slave

stations.

Regarding claims 9 and 15, the combined system of Riley'539 and Sakagami'525

discloses all aspects of the claimed invention set forth in the rejection of Claim 8 as described

above, and Riley'539 further teaches wherein said message includes a read request, said step

of accessing a register in said data link module further comprises the step of reading a value

from said specified register as a read value (see FIG. 15, Parallel Shift Register 590 and 588;

see FIG. 2A, Word Extender circuit 430; col. 21, line 1 to col. 22, line 40; note that the

master clock signal instructs/requests to retrieve/copy/read the data from the registers and

transmits the data to the data bus. Each retrieved/copied/read data must be presented by a

number/value/unique-entry (i.e. time slot number, frame number, or a particular state/status

of the clock) in order to access, retrieve and transmit them to the dedicated output data link.

Note that when the instruction causes the data link module to retrieve/copy/place/move the

data, it is a read request, and a number/value/unique-entry associated with such instruction is

the read value).

Regarding claims 11 and 17, the combined system of Riley'539 and Sakagami'525

discloses all aspects of the claimed invention set forth in the rejection of Claim 8 as described

above, and Riley'539 further teaches wherein said message segment includes a write request,

said step of accessing a register in said data link module further comprises the step of writing

said message data segment to said specified register (see FIG. 15, Shift Registers 590 and

588; see col. 3 55-65; note that in response to the master clock request/instruct signal, the

data link module stores the associated data in dedicated register. Thus, the request/instruction

signal is the write signal message request.)

Sakagami'525 further discloses wherein said message includes a request (see FIG. 3,

HD, ADS, SLP and AP; see col. 6, line 5-64; note that when the slave station receives the

DFa frame with Rx logic value 0 and parity bit value 1 from the master station, it performs

the tasks accordingly).

In view of this, having the system of Riley'539 and then given the teaching of

Sakagami'525, it would have been obvious to one having ordinary skill in the art at the time

the invention was made to modify the system of Riley'539, by further performing tasks

according to the headers/control requests/bits, as taught by Sakagami'525, for the same

motivation as stated above in Claim 8.

Regarding Claim 13, Riley'539 discloses a data link module (see FIG. 1, Data Link

Module 32) connected to a data bus (see FIG. 1, data bus 46) and a master clock line (see

FIG. 1, master clock bus 44) for use in a bit level network system having multiple data link

modules (see FIG. 1, plurality of Data Link modules 32; col. 6, line 40-52; note the system is

able to transfer the multi-bits of data), the master clock line for generating a predetermined

number of time slots for a complete multiplexed channel (see FIG. 21, Time slots 85; see col.

5, line 2-65; note that the master clocks configures the time slots to a frame),

each time slot on the complete multiplexed channel associated with an address

location of at least one data link module or a data bit on the data bus (see FIG. 21, Frame

Identifiers/addresses in plurality of frames/messages; see col. 5, line 2-65; see col. 16, line 54

and col.17, line 24. Note that after multiplexing the time slots, each frame is given a

predefined/unique frame number associated with a data link module), said data link module

comprising:

means for interfacing with either an input device (see FIG. 1, Input device 50) or an

output device (see FIG. 1, Output device 54);

means for receiving data from the data bus at a predetermined time slot on a first

multiplexed channel (see FIG. 2A and 2B, Integrated circuit 80 and input terminals and

output terminals; see col. 7, line 50 to col. 8, line 25; note that the data signal is received in

the input data link module from the bus. Channel A inputs/receives the data signal at a

particular time slot according to the master clock);

means for sending data to the data bus during said predetermined time slot on a second multiplexed channel (see FIG. 2A and 2B, Integrated circuit 80 and input terminals and output terminals; see col. 7, line 50 to col. 8, line 25; note that the data signal is received in the input data link module from the bus. Channel B outputs/shifts the data signal at a particular time slot according to the master clock);

means for processing said data (see FIG. 16, Integrated circuit 80 which is in communication with conductors (i.e. Data bus 46 and common bus 48) in order to process the data signal);

means for storing said data (see FIG. 15, Shift Registers 590 and 588; see col. 3 55-65; note that in response to the master clock request/instruct signal, the data link module stores the associated data in the specific corresponding registers); and

means for retrieving said data (see FIG. 15, Shift Registers 590 and 588, and FIG. 1, data bus 46 and clock bus 44; see col. 3, line 65-67; note that in response to the master clock request/instruct signal, the data link module retrieves/recalls the stored associated data for transmission to the data bus.)

Riley'539 does not explicitly disclose said message including a command segment and a data segment.

However, the above-mentioned claimed limitations are taught by Sakagami'525. In particular, Sakagami'525 teaches said message including a command segment (see FIG. 3, header/control information bits: HD, ADS, SLP, and AP) and a data segment (see FIG. 3, data information bits: Rx). Also see col. 6, line 16-64.

In view of this, having the system of Riley'539 and then given the teaching of

Sakagami'525, it would have been obvious to one having ordinary skill in the art at the time

the invention was made to modify the system of Riley'539, by providing a data frame which

consists of both command/control/header bits and data bits, as taught by Sakagami'525. The

motivation to combine is to obtain the advantages/benefits taught by Sakagami'525 since

Sakagami'525 states at col. 3, line 5-40 that such modification would improve the

communication and exchange of information between a master station and slave stations.

Allowable Subject Matter

3. Claims 10, 12,16 and 18 are objected to as being dependent upon a rejected base claim, but

would be allowable if rewritten in independent form including all of the limitations of the

base claim and any intervening claims.

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this

Office action. Accordingly, **THIS ACTION IS MADE FINAL.** See MPEP § 706.07(a).

Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE

MONTHS from the mailing date of this action. In the event a first reply is filed within TWO

MONTHS of the mailing date of this final action and the advisory action is not mailed until after

the end of the THREE-MONTH shortened statutory period, then the shortened statutory period

will expire on the date the advisory action is mailed, and any extension fee pursuant to 37

CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ian N Moore whose telephone number is 571-272-3085. The examiner can normally be reached on M-F: 9-5.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Ken Vanderpuye can be reached on 571-272-3078. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

INM
10/18/04

BRIAN NGUYEN
PRIMARY EXAMINER